AMENDMENT TO CLAIMS

The listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-36 (cancelled)

Claim 37 (Currently Amended) A method, comprising:

assigning a group of instructions selected from a plurality of groups of instructions partitioned from a program, to a subset of interconnected computation nodes preselected from a plurality of interconnected computation nodes, the instructions having respective associated operands, and each computation node includes a store and an execution unit having one or more arithmetic logic units, floating point units, memory address units, or branch units;

loading a subset of instructions of the assigned group of instructions into a frame of buffers comprising the stores disposed on the preselected subset of interconnected ~~preselected~~ computation nodes having been assigned the group of instructions, wherein the loading is performed prior to the associated operands of the subset of instructions are available;

receiving the respective associated operands of the subset of instructions by the preselected subset of computation nodes, including a first computation node of the preselected subset of computation nodes directly receiving a first associated operand of a first instruction loaded into the first ~~preselected~~ computation node, from a second computation node of the preselected subset of computation nodes, wherein the first computation node has an input port capable of being coupled to the second computation node to enable the directly receiving of the first associated operand; and

executing the subset of instructions as each one of the instructions in the subset of instructions loaded into the frame of buffers receives the respective associated operands for execution.

Claim 38 (Currently amended) The method of claim 37, further comprising storing the first associated operand in a first store of the first computation node, wherein the first store is coupled to the input port, storing the first instruction in a second store of the first computation node,

wherein the second store is coupled to an instruction sequencer, , matching the first associated operand with the first instruction by an instruction wakeup unit, executing the first instruction by an execution unit of the first computation node using at least the first associated operand to produce output data, and routing the output data to an output port of the first computation node, wherein the output port is capable of being coupled to a third of the preselected subset of interconnected computation nodes to directly provide the output data to the third ~~preselected~~ computation node.

Claim 39 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is a basic block.

Claim 40 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is a hyperblock.

Claim 41 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is a superblock.

Claim 42 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is an instruction trace constructed by a hardware trace construction unit at run time.

Claim 43 (Currently Amended) The method of claim 37, wherein loading the subset of instructions into a frame of buffers comprising the stores disposed on the preselected subset of interconnected ~~preselected~~ computation nodes includes:

sending at least two instructions selected from the group of instructions from an instruction sequencer to a selected ~~computation node included in~~ one of the preselected subset of interconnected ~~preselected~~ computation nodes for storage in a store of the selected computation node, wherein the sending is performed prior to the at least two instructions having all necessary associated operands for execution.

Claim 44 (Currently Amended) The method of claim 37, wherein executing the subset of instructions loaded into the frame of buffers as each one of the instructions in the subset of instructions receives the respective associated operands for execution includes:

matching at least one instruction selected from the subset of instructions with at least one operand ~~received from an other computation node included in the subset of interconnected preselected computation nodes~~.

Claim 45 (Cancelled)

Claim 46 (Currently Amended) The method of claim 37, further comprising concurrently assigning another group of instructions selected from the plurality of groups of instructions to another ~~or the same~~preselected subset of interconnected ~~preselected~~ computation nodes for concurrent execution using ~~one or more~~ another frames of buffers comprising stores disposed on the another ~~or same~~ preselected subset of interconnected ~~preselected~~ computation nodes, wherein the two groups of instructions are capable of concurrent execution.

Claim 47 (Currently Amended) An article comprising a ~~machine~~computer-accessible medium having ~~machine~~ computer executable ~~instructions~~ codes stored therein, ~~if executed,~~ configured to enable a machine , in response to execution of the codes by the machine, to:

assign ~~a subset of~~ a group of instructions selected from a plurality of groups of instructions partitioned from a program, to a subset of interconnected computation nodes preselected from a plurality of interconnected computation nodes of the machine, the instructions having respective associated operands, and each computation node includes a store and an execution unit having one or more arithmetic logic units, floating point units, memory address units, or branch units; and

load a~~the~~ subset of the~~a~~ group of instructions into a frame of buffers comprising the stores disposed on the preselected subset of interconnected ~~preselected~~ computation nodes, wherein the subset of the group of instructions is loaded into the frame of buffers prior to the respective associated operands of the ~~subset of the group of~~ instructions are available;

wherein the loaded instructions are executed as each one of the instructions receives the respective associated operands for execution,

wherein the receivinge of respective associated operands includes at least a first computation node of the preselected subset of interconnected computation nodes directly receiving a first associated operand of a first instruction from a second computation node of the preselect subset of interconnected computation nodes ~~coupled to the first computation node~~.

Claim 48 (Currently Amended) The article of claim 47, wherein the ~~machine~~ computer executable ~~instructions~~codes, ~~if executed,~~ further enable the machine, in response to execution of the codes by the machine, to partition the program into the plurality of groups of instructions during compilation of the program.

Claim 49 (Currently Amended) The article of claim 47, wherein the ~~machine~~ computer executable ~~instructions~~codes, ~~if executed,~~ further enable the machine, in response to execution of the codes by the machine, to partition the program into the plurality of groups of instructions ~~is performed~~ during run-time.

Claim 50 (Currently Amended) The article of claim 47, wherein the ~~machine-accessible~~computer-readable medium further includes ~~instructions~~codes, ~~if executed,~~ configured to enable the machine, in response to execution of the codes by the machine, to statically assign ~~each~~ another group of instructions selected from~~of~~ the plurality of groups of instructions to another preselected subset of interconnected ~~preselected~~ computation nodes ~~preselected from a~~ of the plurality of interconnected computation nodes for execution.

Claim 51 (Cancelled)

Claim 52 (Currently amended) The article of claim 47, wherein the ~~machine-accessible~~computer-readable medium further includes ~~instructions~~codes, ~~if executed,~~ configured to enable the machine, in response to execution of the codes by the machine, to generate a wakeup token to

reserve an output data channel of the second computation node to directly route the first associated operand from the second computation node to the first computation node.

Claim 53 (Currently Amended) The article of claim 47, wherein the ~~machine-accessible~~computer-readable medium further includes ~~instructions~~ codes, ~~if executed,~~ configured to enable the machine, in response to execution of the codes by the machine, to repeat said loading until the entire group of instructions are executed, ~~and~~ to detect execution termination of the group of instructions ~~including an output having architecturally visible data~~; and to commit~~ting the~~ architecturally visible data resulted from execution of the group of instructions to a register file.

Claim 54 (Currently Amended) The article of claim 47, wherein the ~~machine-accessible~~computer-readable medium further includes ~~instructions~~ codes, ~~if executed,~~ configured to enable the machine, in response to execution of the codes by the machine, to repeat said loading until the entire group of instructions are executed, ~~and~~ to detect execution termination of the group of instructions ~~including an output having architecturally visible data~~; and to commit~~ting the~~ architecturally visible data resulted from execution of the group of instructions to a memory.

Claim 55 (Currently Amended) The article of claim 47, wherein the ~~machine-accessible~~computer-readable medium further includes ~~instructions~~codes, ~~if executed,~~ configured to enable the machine, in response to execution of the codes by the machine, to route an output datum arising from executing one of the subset of instructions to a consumer node included in the ~~plurality~~ preselected subset of interconnected ~~preselected~~ computation nodes, wherein ~~the~~an address of the consumer node is included in a token associated with at least one instruction included in the subset of instructions.

Claim 56 (Previously presented) The method of claim 37 further comprising repeating said loading and executing until the entire group of instructions have been executed.

Claim 57 (Currently amended) An apparatus, comprising:

a plurality of interconnected computation nodes, each computation node including a store and an execution unit having one or more arithmetic logic units, floating point units, memory address units, or branch units; and

a storage medium coupled to athe processor and configured to have first instructions stored therein to be executed by the processor, wherein the first instructions are configured to enable the apparatus, in response to execution of the first instructions, to:

assign a group of second instructions selected from a plurality of groups of second instructions partitioned from a program to a preselected subset of the plurality of interconnected computation nodes, the second instructions having respective associated operands; and

causing a subset ~~of the second instructions~~ of the assigned group of second instructions to be loaded into a frame of buffers comprising the stores disposed on the preselect subset of interconnected computation nodes having been assigned the group of second instructions, wherein the loading is caused prior to the respective associated operands of the subset of the second instruction are available, wherein at least a first of the associated operands of a first of the second instructions loaded into a first computation node of the preselected subset of the interconnected computation nodes is directly received from a second computation node of the preselected subset of the interconnected computation nodes, wherein the subset of second instructions are executed as each one of the ~~instructions in the~~ subset of second instructions loaded into the frame of buffers receives the respective associated operands for execution.

Claim 58 (Currently Amended) The apparatus of claim 57, wherein at least one of the plurality of groups of the second instructions is a selected of one a basic block, a hyperblock or a superblock.

Claim 59 (Cancelled)

Claim 60 (Currently amended) A system, comprising:

a plurality of interconnected computing nodes configured to be pre-selectable to cooperatively execute ~~a subset of~~ a group of instructions, wherein the group of instructions is one of a plurality groups of instructions partitioned from a program and the instructions have respective associated operands;

wherein ~~individual~~ a first computation node of the plurality of interconnected computing nodes includes:

a computing resource including an execution unit configured to execute instructions, the execution unit having one or more arithmetic logic units, floating point units, memory address units, or branch units; and

an interconnect resource coupled to the computing resource to enable the first computing node to ~~cooperate~~ be preselected with ~~the other~~at least a second of the plurality of interconnected computation nodes to execute the group of instructions by successively executing subsets of the group of instructions;

wherein the interconnect resource includes:

~~at least one~~an input port capable of directly coupling the computing resource to ~~at least a first other preselected~~ the second computation node ~~included in the plurality of interconnected preselected computation nodes~~, and the input port is configured to receive input data,

a first store coupled to the ~~at least one~~ input port, and configured to store the input data,

a second store coupled to the execution unit, and configured to receive and store ~~at least one~~an instruction of a subset of the group of instructions, the second store being a part of a frame of buffers spanning the preselected ~~plurality~~ subset of interconnected ~~preselected~~ computation nodes to store the~~a~~ subset of the group of instructions loaded into the frame of buffers, wherein the subset of instructions are loaded prior to respective ~~the~~ associated operands of the ~~the subgroup~~ subset of the group of instructions are available,

an instruction wakeup unit to match the input data to the ~~at least one~~ stored instruction,

an output port coupled to the execution unit and capable of directly coupling the computing resource to the~~a~~ second or a third of the ~~other~~ preselected subset of interconnected computation node~~s~~ ~~included in the plurality of interconnected preselected computation nodes~~, and

a router coupled to the execution unit, and configured to direct an output data of the execution unit to the output port for direct provision to one of the second ~~other~~ or third computation node.